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(54) **Synchronous digital communication transmission system with hierarchical synchronization network**

(57) In synchronous digital communication transmissions in which a synchronization quality indicator (SSM) is used, synchronization loops (timing loops) may under some circumstances form.

In order to avoid such timing loops, a synchronous digital communications transmission system with network elements (NE11, ..., NE33) is indicated in which two classes (top, bottom) are established for interface devices (S_1, ..., S_x, ..., S_{x+i}).

Figure 1

Auswaleinrichtung	selector device
Steuereinrichtung	control device
Taktgenerator	clock generator

Description

The invention concerns a synchronous digital telecommunications transmission system according to the precharacterizing clause of the patent claim and a network element according to the precharacterizing clause of Claim 6 for a synchronous digital telecommunications system.

A synchronous digital telecommunications system works, by way of example, according to a standard for synchronous digital hierarchy (SDH/SONET standard). In such a digital transmission system, individual network elements are connected to each other through various transmission media (for example, copper cable, optical waveguides, or radio link).

A connection of a network element to a transmission medium takes place through interface devices (network node interfaces) which are known by way of example from ITU-T recommendations G.703 and G.957. In recommendation G.703, specifications of electrical properties of such interface devices are given and in recommendation G.957, specifications of optical properties of network interface nodes are given. In a interface device which is connected to an optical waveguide, incoming optical signals, by way of example, are converted by an optoelectrical converter into electrical signals.

A network element is, by way of example, an exchange for a public telephone network or a crossconnect or and add/drop multiplexer. A switching principle used in the exchange makes it necessary for all exchanges in a system to work together synchronously. The article by M. Wolf et al, "Synchronisierung und Timing" (Synchronization and Timing), Elektrisches Nachrichtenwesen (Alcatel), 4th Quarter 1993, pages 349-358, gives an overview of how exchanges can be synchronized.

Mentioned there are two methods for synchronization of network elements: master/slave synchronization and mutual synchronization.

In the master/slave method, a single primary reference clock is used for synchronizing a first hierarchical level of nodes. These nodes transfer their derived clocks to the nodes of a following level, and so forth. In the method of mutual synchronization, all nodes are equivalently connected to each other through the existing digital connections. In each node, an average phase value is calculated from the incoming clock signals and an internal clock of its own.

In the master/slave method, a hierarchal synchronization system is thus present. In a system according to the standard for synchronous digital hierarchy (SDH), a frame is established which in a multiplex segment has a section designated as SOH (section overhead). In this SOH, a synchronization quality indicator can be transmitted for which bits 5 through 8 of the S1 byte are specified. (See by way of example ITU-T recommendation G 707, G 708, or G 709).

This synchronization quality indicator indicates a quality class of a transmitted standardized reference clock and provides a powerful autonomous function for improvement of the quality management of synchronization. The synchronization quality indicator is generally known as "synchronization status message," and is designated below with SSM. Set through bits 5 through 8 of the S1 byte is among other things standardized reference clock G.811, G.812 according to ITU-T or a message "Don't use for synchronization," which is referred to below as DNU.

Known from a working document by B. Neihoff "More on Synchronization Status Message Problems," ETS/TM3/WG6, Working Document 22, Oslo, 25-29 October 1993, is that in the use of SSM, problems can arise. Among these are synchronization loops (timing loops) which arise if a network element (SDXC) loses a selected source, as in Figure 2 of the working document, and

with the aid of a selection procedure (synchronization source selection algorithm, SSSA) selects a different reference source. It is also mentioned that such synchronization loops can occur in any network arrangement in which two bi-directional SSM routes end in the same network element and are also generated there. In the working document it is suggested as a solution to the problem that "enable/disable" functions be defined.

The invention is based on the task of suggesting another digital telecommunications system in which no synchronization loops can arise. A digital telecommunications system which solves this task is the object of Patent Claim 1. In addition, the invention is based on the task of suggesting a network element for such a telecommunications system. A network element which solves this task is the object of Patent Claim 6.

Advantageous embodiments of the invention are given in the subclaims.

The invention will be explained in greater detail with the aid of drawings.

Figure 1 shows a network element in which two priority classes are established for node interfaces, and

Figure 2 shows a digital telecommunications transmission system with nine network elements.

Shown in Figure 1 is a network element which by way of example is part of a telecommunications transmission system which works according to the standard for synchronous digital hierarchy (SDH).

In such a digital telecommunications system, the network elements are connected to each other by way of example through copper cable and/or optical waveguides. The network element, which for example is a crossconnect, has a number of interface devices $S_1,\ldots, S_x, \ldots, S_{x+i}$.

In Figure 1, six interface devices S_1, S_2, S_x, S_{x+1}, S_{x+2}, S_{x+i} are drawn in; for clarity, three interface devices S_1, S_2, S_x are situated on one side of the network, which will be designated below as the top side, and three interface devices S_{x+1}, S_{x+2}, S_{x+i} are situated on the opposite side, which will be designated below as the bottom side.

At each interface device S_1, S_2, S_x of the top side, an SSM arrives which is designated in accordance with the interface devices S_1, S_2, S_x as SSM_1, SSM_2, SSM_x. From each interface device S_1, S_2, S_x, an SSM can also be sent out, for example with the report DNU. In Figure 1 the directions of the SSM are drawn in through arrows with corresponding direction to interface devices S_1, S_2, S_x.

The network element also has a selector device 1 in which a clock filter is contained, a clock generator 6, and a control device 7. Each interface device S_1, S_2, S_x is connected to selector 1 through a connection 3, 2, 5. By this means, the clocks from STM-N signals arriving at interface devices S_1, S_2, S_x are brought to selector 1. In addition, each interface device S_1, S_2, S_x is connected to control device 7 through a connection 8, 9, 10. SSM_1, SSM_2, SSM_x are brought through these connections 8, 9, 10 to control device 7. Control device 7 in turn is connected through a control line 12 to selector 1, and through a connection 2 to clock generator 6. Selector 1 is connected through a connection 4 to clock generator 6.

Control device 7 is connected to interface devices S_{x+1}, S_{x+2}, S_{x+i} of the bottom side through a connection 13. At an output 14 of clock generator 6, the clock emerges which is relayed to other

network elements. For this purpose, output 14 is connected to each interface device S_1, ..., S_x, ..., S_{x+i}; for simplification, this is suggested in Figure 1 through an arrow drawn in at output 14.

Concerning the function of the individual components:

The clock filter present in evaluation device 1 is specified through ITU recommendation G.812 or G81s. It has the task of filtering out clock disturbances (jitter and wander). A further task of the clock filter is to maintain the frequency of its output signal as constant as possible upon loss of its input signal.

Control device 7 evaluates incoming SSM, SSM_2, SSM_3 and determines from this an interface device S_1, S_2, S_x as clock reference source. Selector device 1 is then controlled by control device 7 such that the clock of the clock reference source is relayed to clock generator 6. Clock generator 6 by way of example is a phase locked loop (PLL) which following synchronization to the clock coming from evaluation device 6 relays this clock through output 14. If synchronization of clock generator 6 is not possible because, by way of example, too much noise accompanies the clock or because the clock has been lost, clock generator 6 gives control device 7 a message to this effect. Such a message causes, for example, the network element to pass into a holdover condition. Control device 7 generates an SSM which corresponds to the current condition of the network element. This SSM can be one of the SSM_1, SSM_2, SSM_x received at interface devices S_1, S_2, S_x of the top side, but it can also be a new SSM generated by control device 7.

Interface devices S_{x+1}, S_{x+2}, S_{x+i} of the bottom side each relay the selected or generated SSM; arriving SSMs in contrast are ignored. The directions of the SSM at interface devices S_{x+1}, S_{x+2}, S_{x+i} are also drawn in with arrows with corresponding direction. Two classes (top, bottom) are established for this network element for interface devices S_1, ..., S_x, ..., S_{x+i}: Interface devices S_1,

S_2, S_x of the top side have the class "top" and interface devices S_{x+1}, S_{x+2}, S_{x+i} of the bottom side have the class "bottom." Classes "top, bottom (abbreviated: bot)" are drawn in Figure 1 at interface devices S_1, ..., S_x, ...S_{x+i}.

Interface devices S_1, S_2, S_x of the class "top" represent possible clock reference sources from which one is selected through control device 7. This means that connected to interface devices S_1, S_2, S_x, of this class "top," interface devices of one or more other network elements, the SSM of which are theoretically accepted for synchronization. Interface devices S_{x+1}, S_{x+2}, S_{x+i} of the class "bottom" ignore, as already mentioned, arriving SSMs, i.e., SSMs arriving from other network elements are not used for synchronization.

With such network elements as described above, a synchronization network can be created even in a non-hierarchical transmission and switching system. It can be specified through specification of the classes "top, bottom" of an interface device whether the network element may synchronize another network element or not.

Shown in Figure 2 is an exemplary hierarchical synchronization network with nine network elements NE11 ... NE33. These network elements NE11 ... NE33 are depicted in the form of a grid (3x3 matrix) with the grid points depicting the idealized geographic locations of network elements NE11 ... NE33 and the grid lines representing the cable and/or radio connections between the network elements. At network elements NE11, NE13, NE32 a reference clock is fed into the hierarchical synchronization network. The reference clock (the "master clock") is generated by a reference clock source which by way of example is a cesium clock which has a clock stability of 10^{-11}. In Figure 2, network elements NE11, NE13, NE32 are depicted as solid circles and the remaining network elements NE12, NE21, ..., NE31, NE33, which do not have a

reference clock source, as unfilled circles. At the individual network elements NE11, ... NE33, the classes "top" and "bottom" are indicated.

Network elements NE11, NE13, NE32 have only interface devices with the class "bottom"; they cannot be synchronized by other network elements.

Network element NE21 accepts only a clock coming from network element NE11 (class "top") and ignores SSMs which come from network elements NE22, NE31 (class "bottom").

The remaining synchronizing devices for the individual network elements can be derived from Figure 2 so that explanation of them can be omitted here.

Patent Claims

1. Synchronous digital communications transmission system with a number of network elements (NE11 ... NE33) which each have several interface devices (S_1, ..., S_x, ..., S_{x+i}) and with at least one transmission medium, through which the network elements (NE11 ... NE33) are connected to each other, characterized in that the interface devices (S_1, ..., S_x, ..., S_{x+i}) of a network element (NE11 ... NE33) are divided into two classes (top, bottom), on the basis of which a synchronization hierarchy is established.

2. Network element for a synchronous digital communications transmission system with several interface devices (S_1, ..., S_x, ..., S_{x+i}), characterized in that the interface devices (S_1, ..., S_x, ..., S_{x+i}) are divided into two classes (top, bottom) on the basis of which a synchronization hierarchy is established in the synchronous digital communications transmission system.

3. Synchronous digital communications system according to Claim 1 or network element according to Claim 2 characterized in that the interface devices (S_1, ..., S_x) of the first class (top) are possible clock reference sources.

4. Synchronous digital communications system according to Claim 1 or network element according to Claim 2 characterized in that the interface devices (S_{x+1}, ..., S_{x+i}) of the second class (bot) ignore arriving synchronization signals.

5. Synchronous digital communications system according to Claim 3 characterized in that the network elements (NE11, ..., NE33) have a selector device (1) and a control device (7) connected to the selector device (1), each of which are connected to the interface devices (S_1, ..., S_x) of the first class (top); that the control device (7) evaluates synchronization quality indicators (SSM_1, ..., SSM_x) arriving at the interface devices (S_1, ..., S_x) and selects an interface device (S_1, ..., S_x) as clock reference source, the clock of which the selector device (1) sends to a clock generator (6); that the clock generator (6) checks the clock, and relays it to the interface devices (S_1, ..., S_x, ..., S_{x+i}); and that the control device (7) relays one of the synchronization quality indicators (SSM_1, ..., SSM_x) or one of the synchronization quality indicators generated by it to the interface devices (S_{x+1}, S_{x+i}) of the second class (bottom).

Figure 1

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European Patent Office | **EUROPEAN SEARCH REPORT** | Number of the Application EP 95 12 0268

RELEVANT DOCUMENTS			
Category	Identification of the document including, to the extent necessary, the critical portions	Concerns Claim	Classification of the application (Int. Cl. [6])
Y	IEEE TRANSACTIONS ON COMMUNICATIONS, AUG. 1980, USA, Vol.. COM-28, No. 8, pt. 1, ISSN 0090-6778, pages 1234-1244, XP000577347 STOVER H A: "Network timing/synchronization for defense communications" * Page 1234, right column, paragraph 3 * * Page 1235, right column, paragraph 2* * Page 1236, left column, last paragraph – right column, paragraph 2* * Page 1238, right column, last paragraph* ---	1-5	H04J3/06
Y	BRITISH TELECOMMUNICATIONS ENGINEERING, Vol. 12, No. Part 03, October 1, 1993 LONDON, GB, Pages 207-215, XP000405932 ANDREWS M ET AL: "BT NORTHERN IRELAND STAR SDH NETWORK NISTAR: * Page 210, right column, paragraph 1-page 211, left column, paragraph 3; figures 5, 6* ---	1-5	Field searched (Int. Cl[6]) H04J
A	REVIEW OF THE ELECTRICAL COMMUNICATION LABORATORIES, JULY-AUG. 1977, JAPAN, Vol. 25, No. 7-8, ISSN 0029-067X, Pages 717-729, XP002010777 EGAWA T ET AL: "Network synchronization system for DDX-2" *Page 722, left column, paragraph 4.1.3; figure 5* --- -/--	1,2	
This search report was prepared for all patent claims.			

Search Office	Ending date of the search	Examiner
THE HAGUE	August 22, 1996	Pieper, T

	CATEGORY OF CITED DOCUMENTS		
X	Of particular relevance when considered alone	T	Theories or principles on which the invention is based
Y	Of particular relevance when combined with another publication of the same category	E	Older patent document which however was not published until after the filing date
A	Technological background	D	Document cited in the application
O	Non-written disclosure	L	Document cited for other reasons
P	Interim literature	.....	
		&	Member of the same patent family, conforming document

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RELEVANT DOCUMENTS			
Category	Identification of the document including, to the extent necessary, the critical portions	Concerns Claim	Classification of the application (Int. Cl. [6])
D,A	ELECTRICAL COMMUNICATION, October 1, 1993, Pages 349-358, XP000425700 POWELL W E ET AL: "SYNCHRONIZATION AND TIMING OF SDH NETWORKS" *Page 349, right column, last paragraph – page 350, middle column, paragraph 1; figures 1, 2* ----	1,2,5	
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This search report was prepared for all patent claims.			

Search Office	Ending date of the search	Examiner
THE HAGUE	August 22, 1996	Pieper, T

	CATEGORY OF CITED DOCUMENTS		
X	Of particular relevance when considered alone	T	Theories or principles on which the invention is based
Y	Of particular relevance when combined with another publication of the same category	E	Older patent document which however was not published until after the filing date
A	Technological background	D	Document cited in the application
O	Non-written disclosure	L	Document cited for other reasons
P	Interim literature		.....
		&	Member of the same patent family, conforming document